RV(RELIABILITY VERIFICATION) AUTOMATION TO IMPROVE EXECUTION EFFICIENCY

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1. Motivation

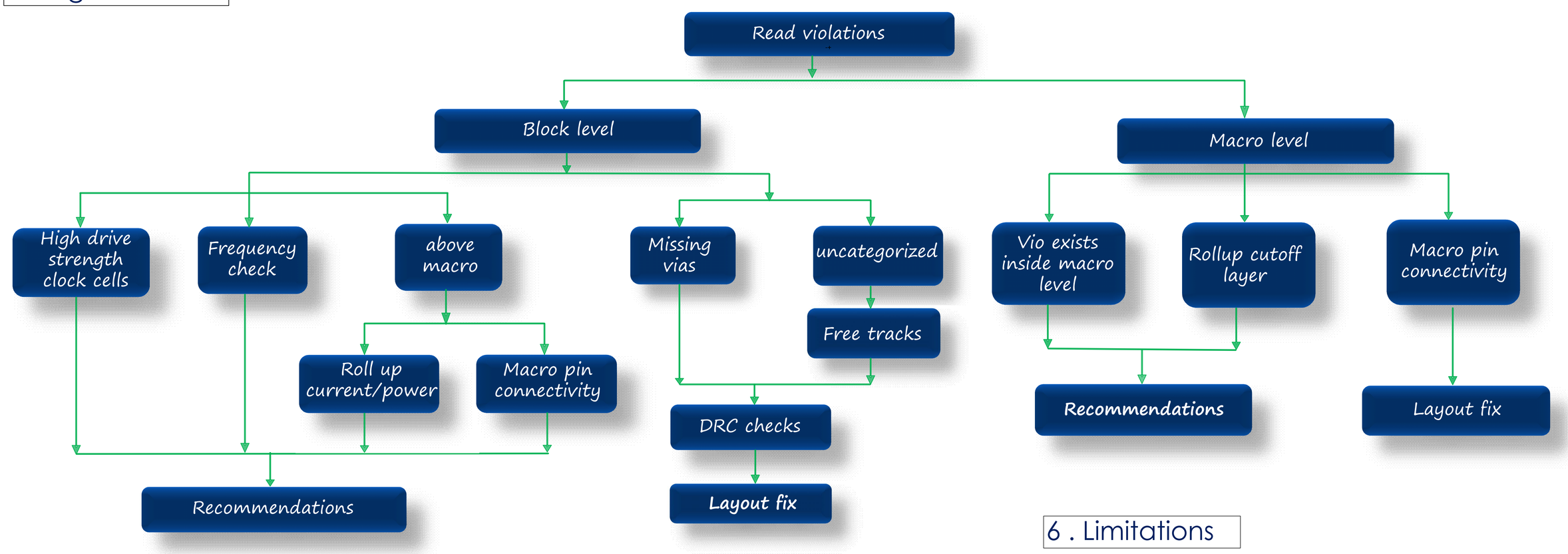
- *Reliability Verification (RV-EM and IR) is typically a difficult and often procrastinated item to Physical design/structural design convergence.*
- *RV Challenges:*
- *High turn around time*
- *Needs good tool, methodology & Design knowledge*
- *Several layout iterations*
- *Deprioritized till end milestone since it requires power & ground shorts clean layout and it is not performance critical*

Effort table	
IP	Approx. efforts for RV Clean Up (in weeks)
DDRIO	2
UPI	3
HBMIO	3
GPIO	1

2 . Main Idea

. An automation has been proposed and built, which enables the engineers to converge the design quickly by automating the RV analysis & implementing DRC & timing aware layout fixes.
. The automation reduces the iterations and speeds up handoff between the RV, design and layout engineer
. The algorithm categorizes all the violations & provides recommendations based on
. Input collateral issues
. RV aware design recommendations
. Project level waivable violations
. Violations with simple layout fixes
. Remaining violations which requires user attention
. Examples of input collateral issues are incorrect timing information, rollup cut-off layer, toggle rate, etc.
. RV aware design recommendations include, high drive strength/clock cell spreading, addressing high local temperatures, etc.
. Also, provides waivers with good description where a global waiver is applicable thus reducing the effective violation count while keeping standard waiver language
. Fixes the layout if enabled by a switch by keeping other signoff flows in check like LV and Timing.
. Provides a list of violations which the automation is unable to address for the user to investigate.
. The algorithm has features to avoid over fixing by addressing multiple violations with single layout edit.

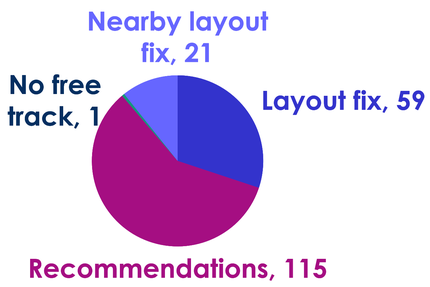
3 . Algorithm



4 . Results

Blocks(project X)	Initial numbers		After using the automation		% of violations addressed
	No. Of Vio	EM violation magnitude	No. of Vio	EM violation magnitude	
Partition 1	335	4	15	1.3	95.52
Partition 2	273	3.2	32	1.7	88.27
Partition 3	82	2.4	11	1.3	86.58
Partition 4	29	3	4	2.3	86.20
Partition 5	184	2.9	50	2.1	72.82

5 . Breakup of addressed violations from a block



6 . Limitations

- *The Algorithm might not be able to address some of the violations in custom/analog power grid with non uniform power grid density.*
- *This Algorithm is limited to EM and IR violations*

7 . Summary

- *Reliability Verification (EM and IR) automation is proposed to improve execution efficiency and reduce Time to Market.*
- *Verified over several IPs & SOCs*
- *Independent of process node/technology*
- *86% higher RV execution efficiency*
- *Improved reviewer efficiency*

- *Next plan is to use Machine Learning algorithms to boost the efficiency to >95%.*